



Doc. Number:

Tentative Specification
Preliminary Specification
Approval Specification

MODEL NO.: N156B6 SUFFIX: L3D

Customer: Lenovo China							
APPROVED BY	SIGNATURE						
Name / Title Note							
Please return 1 copy for your consignature and comments.	firmation with your						

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REVISION HISTORY

Version	Date	Page	Description
3.0	Jul.30, 2010	All	Approval Spec Ver.3.0 was first issued.
3.1	Oct.27,2010	4 &27& 29	1.Update mechanical specifications and drawing for adding EMI tape 2.Update model name from N156BHF-L21 to N156B6-L3D

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156B6-L3D is a 15.6" (15.547" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note		
Screen Size	15.547 diagonal				
Driver Element	a-si TFT active matrix	4	-		
Pixel Number	1366 x R.G.B. x 768	pixel	-		
Pixel Pitch	0.252 (H) x 0.252(V)	mm	-		
Pixel Arrangement	RGB vertical stripe		-		
Display Colors	262,144	color	-		
Transmissive Mode	Normally white	-	-		
Surface Treatment	Hard coating (3H), Glare	-	-		
Luminance, White	220	Cd/m2			
Power Consumption	Power Consumption Total 8.92 W (Max.) @ cell 3.96 W (Max.), BL 4.96 W (Max.)				
Power Consumption Total 9.25 W (Max.) @ cell 4.29 W (Max.), BL 4.96 W (Max.)					

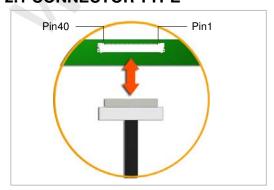
Note (1) The specified power consumption is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 $^{\circ}$ C, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and fv = 60 Hz, whereas mosaic pattern is displayed. Note (2) The specified power consumption is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 $^{\circ}$ C, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and fv = 120 Hz, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	358.9	359.4	359.9	mm	
Module Size	Vertical (V)	209.1	209.6	210.1	mm	(1)
	Thickness (T)	-	5.9	6.2	mm	
Bezel Area	Horizontal	348.13	348.43	348.73	mm	
Dezei Area	Vertical	197.44	197.74	198.04	mm	
Active Area	Horizontal	-	344.232	-	mm	
Active Area	Vertical	-	193.536	-	mm	
Weight		-	495	510	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



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Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12 \ TYCO-5-2069716-3 or equivalent

User's connector Part No: IPEX-20453-040T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

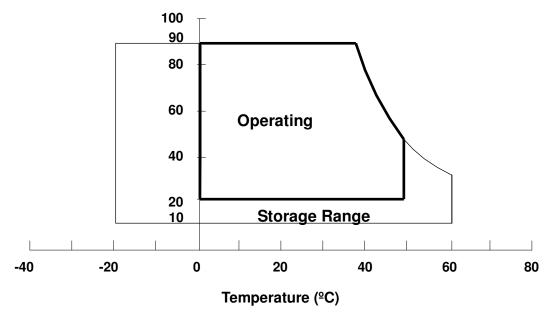
3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Va	lue	Unit	Note	
item	Symbol	Min.	Max.	Offic		
Storage Temperature	T _{ST}	-20	+60	°C	(1)	
Operating Ambient Temperature	T _{OP}	0	+50	∘C	(1), (2)	

- Note (1) (a) 90 %RH Max. (Ta $<= 40 \, {}^{\circ}\text{C}$).
 - (b) Wet-bulb temperature should be 39 $^{\circ}$ C Max. (Ta > 40 $^{\circ}$ C).
 - (c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.





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3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Va	lue	Unit	Note	
Item	Cymbol	Min.	Max.	5	Note	
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)	
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	(1)	
Converter Input Voltage	LED_VCCS	-0.3	25	V		
Converter Control Signal Voltage	LED_PWM,	-0.3	6	V		
Converter Control Signal Voltage	LED_EN	-0.3	6	V		

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

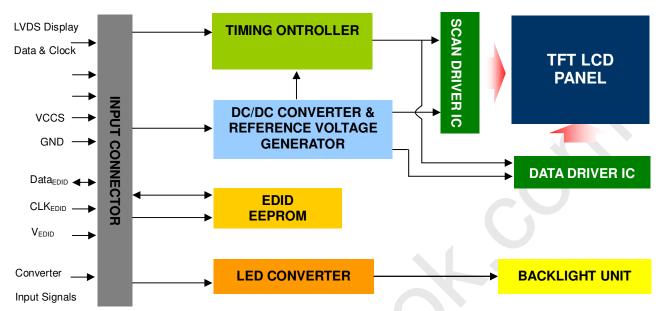
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4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

PIN ASS	SIGNMENT		
Pin	Symbol	Description	Remark
1	Vccs	Power Supply +3.3 V (typical)	
2	Vccs	Power Supply +3.3 V (typical)	
3	Vccs	Power Supply +3.3 V (typical)	
4	V _{EDID}	DDC 3.3V Power	
5	NC	Non-Connection (Reserved for CMO)	
6	CLK _{EDID}	DDC Clock	
7	DATA _{EDID}	DDC Data	
8	RXO0-	LVDS Differential Data Input (Odd)	R0-R5, G0
9	RXO0+	LVDS Differential Data Input (Odd)	no-no, do
10	Vss	Ground	
11	RXO1-	LVDS Differential Data Input (Odd)	G1~G5, B0, B1
12	RXO1+	LVDS Differential Data Input (Odd)	G1*G5, B0, B1
13	Vss	Ground	
14	RXO2-	LVDS Differential Data Input (Odd)	B2-B5,HS,VS, DE
15	RXO2+	LVDS Differential Data Input (Odd)	B2-B3,113, V3, BE
16	Vss	Ground	
17	RXOC-	LVDS Clock Data Input (Odd)	
18	RXOC+	LVDS Clock Data Input (Odd)	
19	Vss	Ground	
20	RxE0-	LVDS Differential Data Input (Even)	R0-R5, G0
21	RxE0+	LVDS Differential Data Input (Even)	
22	Vss	Ground	
23	RxE1-	LVDS Differential Data Input (Even)	G1~G5, B0, B1

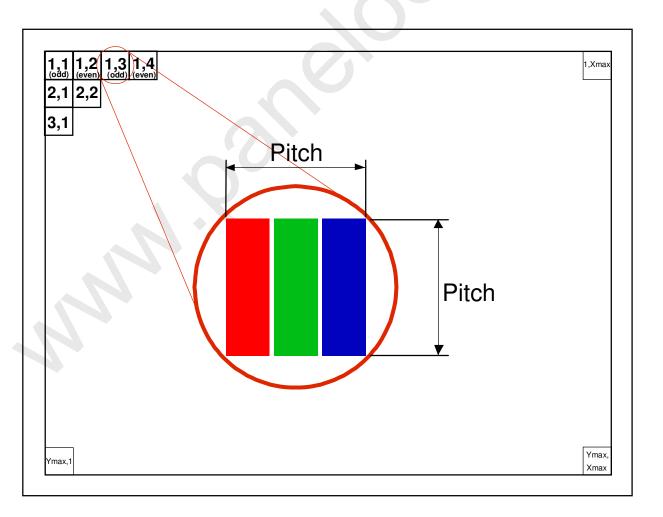
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24	RxE1+	LVDS Differential Data Input (Even)	
25	Vss	Ground	
26	RxE2-	LVDS Differential Data Input (Even)	B2-B5,HS,VS, DE
27	RxE2+	LVDS Differential Data Input (Even)	
28	Vss	Ground	
29	RXEC-	LVDS Clock Data Input (Even)	
30	RXEC+	LVDS Clock Data Input (Even)	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	Non-Connection (Reserved for CMO)	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	Non-Connection (Reserved for CMO)	
38	LED_VCCS	LED Power	
39	LED_VCCS	LED Power	
40	LED_VCCS	LED Power	

Note (1) The first pixel is odd as shown in the following figure.



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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

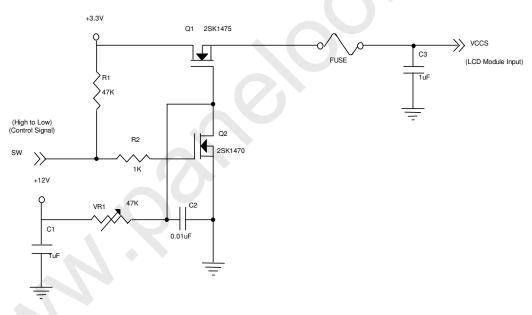
Parameter		Symbol	Value			Unit	Note
		Symbol	Min.	Тур.	Max.	Offic	INOLE
Power Supply Voltage		VCCS	3.2	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	50	-	mV	-
Inrush Current		I _{RUSH}	-	-	1.5	Α	(2)
Power Supply Current	Mosaic	lcc	-	980	1200	mA	60Hz,(3)a
Power Supply Current	Black		-	1070	1300	mA	60Hz,(3)b
Dower Cumply Current	Mosaic		-	1060	1300	mA	120Hz,(3)a
Power Supply Current	Black	lcc	-	1150	1400	mA	120Hz,(3)b

Note (1) The ambient temperature is $Ta = 25 \pm 2$ °C.

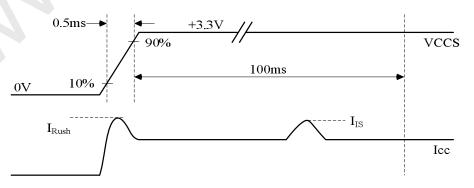
Note (2) I_{RUSH}: the maximum current when VCCS is rising

 $\ensuremath{I_{\text{IS}}}\xspace$ the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



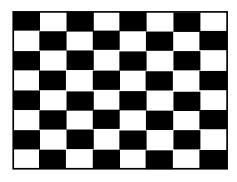
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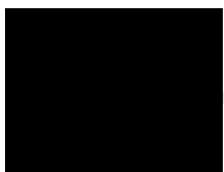
Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 $^{\circ}$ C, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. Black Pattern



Active Area





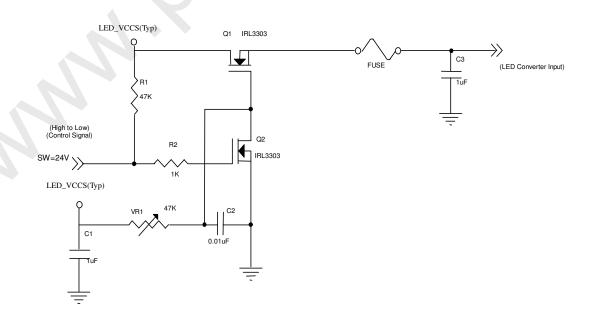
4.3.2 LED CONVERTER SPECIFICATION

Davies		Comple al		Value	l lait	Nata	
Parar	neter	Symbol	Min.	Тур.	Max.	Unit	Note
Converter Input pow	er supply voltage	LED_Vccs	6	12.0	21.0	V	
Converter Inrush Cu	ırrent	ILED _{RUSH}	-	-	1.5	Α	(1)
EN Control I avail	Backlight On		2.3	-	5.0	V	
EN Control Level	Backlight Off		0	-	0.5	V	
DWM Control Lovel	PWM High Level		2.3	-	5.0	V	
PWM Control Level	PWM Low Level		0	-	0.5	V	
PWM Control Duty F	Patio		10	-	100	%	
PWW Control Duty i	hallo		5	-	100	%	(2)
PWM Control F Voltage	Permissive Ripple	VPWM_pp	-		100	mV	
PWM Control Frequ	f _{PWM}	190		2K	Hz	(3)	
LED Power Current LED_VCCS =Ty		ILED	226	339	413	mA	(4)
LED Life Time			15000			Hours	(5)

Note (1) ILED_{RUSH}: the maximum current when LED_VCCS is rising,

 $\ensuremath{\mathsf{ILED}_{\mathsf{IS}}}\xspace$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 \pm 2 $^{\circ}$ C, f_{PWM} = 200 Hz, Duty=100%.



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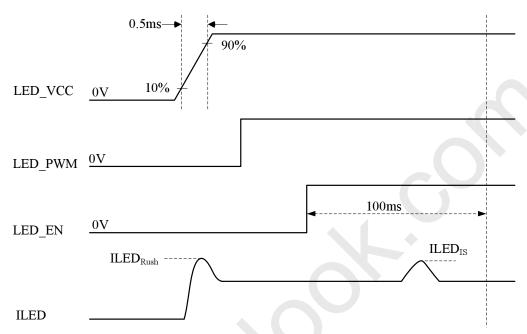




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VLED rising time is 0.5ms



- Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.
- If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency
$$f_{\text{PWM}}$$
 should be in the range
$$(N+0.33)*f \leq f_{\text{PWM}} \leq (N+0.66)*f$$

$$N: \text{Integer} \ \ (N\geq 3)$$

$$f: \text{Frame rate}$$

- Note (4) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 \pm 2 $^{\circ}$ C, f_{PWM} = 200 Hz, Duty=100%.
- Note (5) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 \pm 2oC and IL = 20.0mA (Per EA) until the brightness becomes \leq 50% of its original value.

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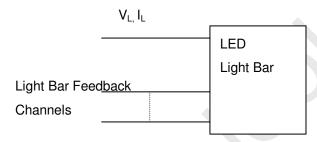


4.3.3 BACKLIGHT UNIT

 $Ta = 25 \pm 2 \,{}^{\circ}C$

Devemeter	Cumahal		Value	l loi+	Nata	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
LED Light Bar Power Supply Voltage	VL	25.2	28.8	31.5	V	(1)(2)(Duty1009()
LED Light Bar Power Supply Current	lL	114	120	126	mA	(1)(2)(Duty100%)
Power Consumption	PL	2.872	3.456	3.969	W	(3)
LED Life Time	L_BL	15000			Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 $^{\circ}$ C and I_L = 20 mA(Per EA) until the brightness becomes \leq 50% of its original value.



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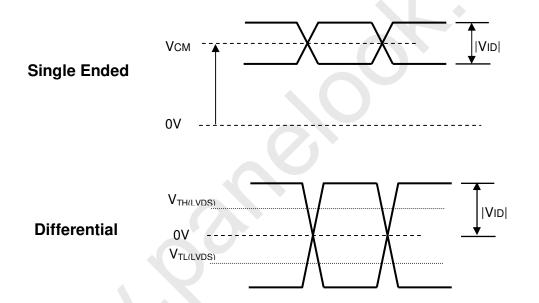
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4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

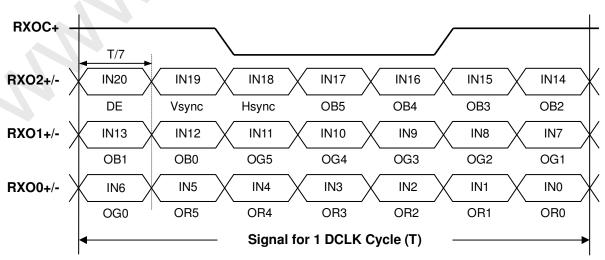
4.4.1 LVDS DC SPECIFICATIONS

Parameter	Symbol		Value	Unit	Note	
	,	Min.	Тур.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V _{CM} =1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V _{CM} =1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	V _{ID}	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.



4.4.2 LVDS DATA FORMAT

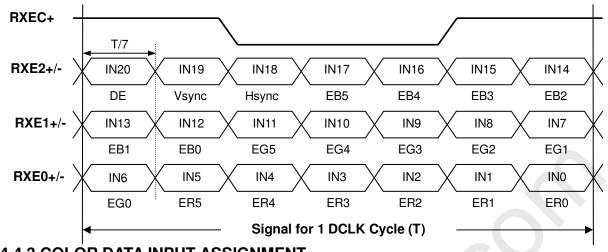


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4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

								I	[Data		al		ı					
	Color				ed						een				-		ue		
	1=	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	В3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	: \	:):)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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4.5 DISPLAY TIMING SPECIFICATIONS

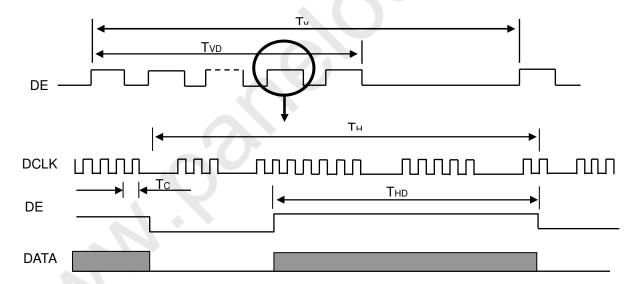
The input signal timing specifications are shown as the following table and timing diagram.

	5 5 1		9				
Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
		1/Tc	36.5	37.7	38.9	MHz	60Hz, (2)
DCLK	Frequency	1/Tc	61.6	62.9	64.1	MHz	100Hz, (2)
DOLK	rrequericy	1/Tc	67.9	69.2	70.4	MHz	110Hz, (2)
		1/Tc	74.2	75.4	76.7	MHz	120Hz, (2)
	Vertical Total Time	TV	798	806	816	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
DE	Vertical Active Blanking Period	TVB	TV-TVD	38	TV-TVD	TH	-
	Horizontal Total Time	TH	1512	1560	1608	Tc	(2)
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	194	TH-THD	Tc	(2)

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



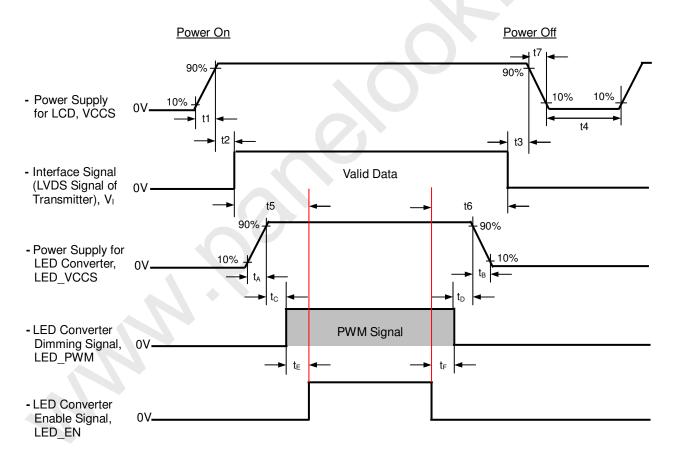




4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Cumphal		Value		l leit	Note
Symbol	Min.	Тур.	Max.	Unit	Note
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	800	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t _A	0.5	-	10	ms	
t _B	0		10	ms	
t _C	10	-	-	ms	
t _D	10	-	-	ms	
t _E	10	-	-	ms	
t⊧	10	-	-	ms	



- Note (1) Please don't plug the interface cable when system is turned on.
- Note (2) Please avoid floating state of the interface signal during signal invalid period.
- Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

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5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit			
Ambient Temperature	Ta	25±2	°C			
Ambient Humidity	На	50±10	%RH			
Supply Voltage	V _{CC}	3.3	V			
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"					
LED Light Bar Input Current	Ι _L	120	mA			

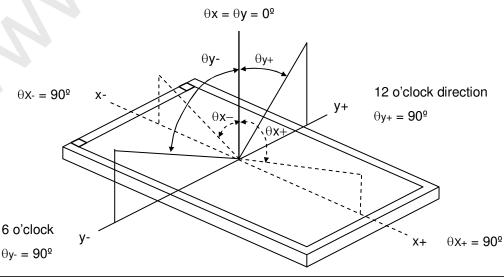
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Iter	m	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		400	500	-	-	(2), (5), (7)
Daananaa Tima		T_R		-	2	4	ms	
Response Time	!	T_F		-	4	8 ms		(3), (7)
Average Luminance of White		Lave		185	220	-	cd/m ²	(4), (6), (7)
	Pod	Rx			0.624		-	
	Red	Ry	$\theta_{x}=0^{\circ}, \ \theta_{Y}=0^{\circ}$		0.342		-	
	Green	Gx	Viewing Normal Angle		0.320		-	
Color		Gy		Тур –	0.588	Typ +	-	(1) (7)
Chromaticity	Blue	Bx		0.03	0.162	0.03	-	(1), (7)
		Ву			0.088		-	
	White	Wx			0.313		-	
	vvriite	Wy			0.329		-	
	Horizontal	θ_{x} +		35	40			
Viewing Angle	попиона	θ_{x} -	OD: 40	35	40	-	D	(4) (5) (7)
	14 ii 15	θ_{Y} +	CR≥10	15	20	-	Deg.	(1),(5), (7)
	Vertical	θ _Y -		35	40	-		
White Variation	of 5 Points	δW_{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	80	-	-	%	(5),(6), (7)

Note (1) Definition of Viewing Angle (θx , θy)

Normal



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Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

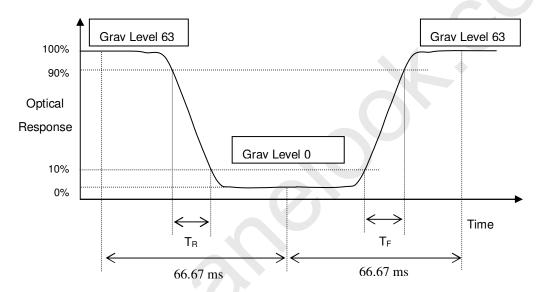
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR(1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5$$

L(x) is corresponding to the luminance of the point X at Figure in Note (6)

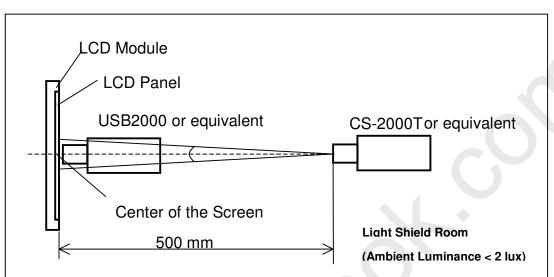


Global LCD Panel Exchange Center

PRODUCT SPECIFICATION

Note (5) Measurement Setup:

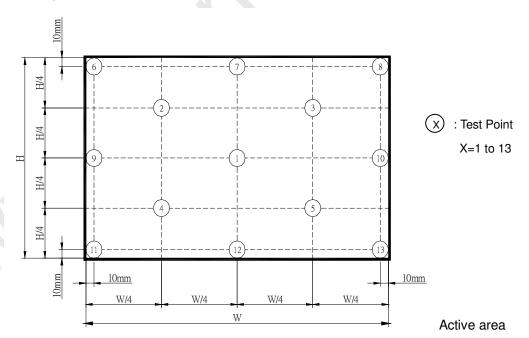
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

 $\delta W_{5p} = \{Minimum [L (1), L (2), L (3), L (4), L (5)] / Maximum [L (1), L (2), L (3), L (4), L (5)]\}*100\%$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour ←→60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	(1) (2)
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330 Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

- Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.
- Note (2) Evaluation should be tested after storage at room temperature for more than two hour
- Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

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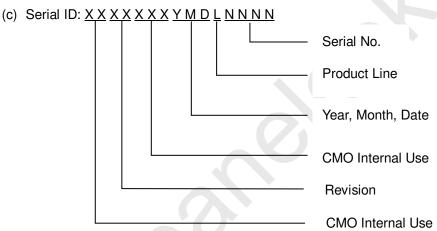
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N156B6 L3D
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

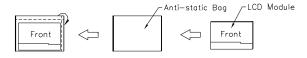
Day: 1~9, A~Y, for 1^{st} to 31^{st} , exclude I , O and U

- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.



7.2 CARTON

- (1) Box Dimensions : 489(L)*382(W)*320(H)
- (2) 20 modules/Carton



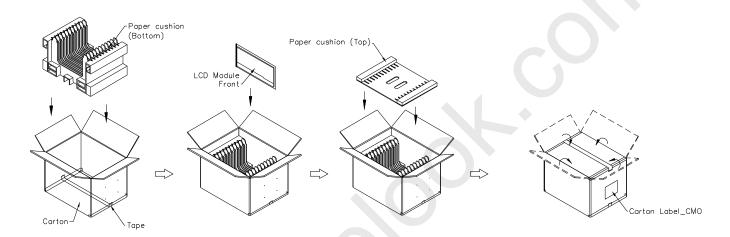


Figure. 10-1 Packing

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7.3 PALLET

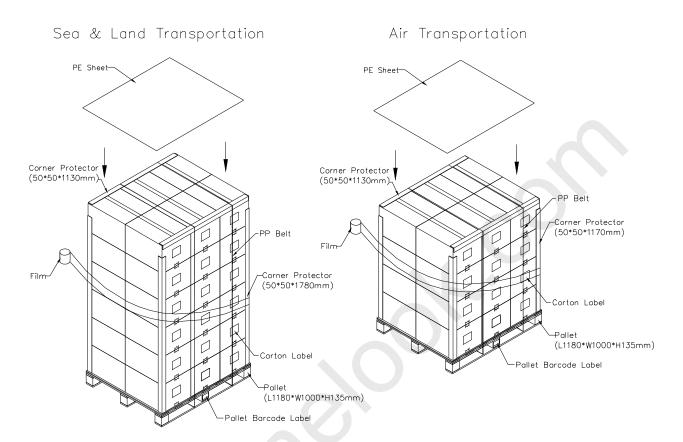


Figure. 7-3 Packing

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8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

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- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

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Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

VESA	Plug & I	Display and FPDI standards.		
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N156B6-L3D)	98	10011000
11	0B	ID product code (hex LSB first; N156B6-L3D)	15	00010101
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed "00H")	09	00001001
17	11	Year of manufacture (fixed "00H")	13	00010011
18	12	EDID structure version # ("1")	01	0000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Max H image size ("34.42cm")	22	00100010
22	16	Max V image size ("19.35cm")	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	D1	11010001
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	F5	11110101
27	1B	Red-x ($Rx = "0.624"$)	93	10010011
28	1C	Red-y (Ry = "0.342")	5D	01011101
29	1D	Green-x (Gx = "0.320")	59	01011001
30	1E	Green-y (Gy = "0.588")	90	10010000
31	1F	Blue-x (Bx = "0.162")	26	00100110
32	20	Blue-y (By = "0.088")	1D	00011101
33	21	White-x (Wx = "0.313")	50	01010000
34	22	White-y (Wy = "0.329")	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

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28 Standard timing ID # 3				0.1	00000004
444 2C Standard timing ID # 4 01 00000001 45 2D Standard timing ID # 5 01 00000001 47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 49 31 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 8 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 Standard timing ID # 8 01 00000001 55 37 # 1 Pixel clock (Nex LSB first) 01 00000001 55 37 # 1 Pixel clock (Nex LSB first) 3A 00111100 55 37 # 1 Pixel clock (Nex LSB first) 3A 00111100 57 39 # 1 H baink ("1366") 56 01010110 <td>+</td> <td></td> <td></td> <td>01</td> <td>00000001</td>	+			01	00000001
45 2D Standard timing ID # 4 01 00000001 46 2E Standard timing ID # 5 01 00000001 47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 49 31 Standard timing ID # 7 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 8 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) F0 1111000 55 37 # 1 Pixel clock (ine LSB first) 3A 00111010 55 38 # 1 H active ("1366") 56 01010110 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H bank ("1366:194") 50 01010000	+		-		
46 2E Standard timing ID # 5 01 00000001 47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 49 31 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) 55 37 # 1 Pixel clock (rex LSB first) 3A 00111010 56 38 # 1 H active ("1865") 56 01010110 57 39 # 1 H blank ("194") C2 1100010 58 3A # 1 H active ("1865") 56 01010110 59 3B # 1 V active ("788") 00 00000000 60 3C # 1 V blank ("38") 26 00100111 61 3D # 1 V active ("788") 30 00110000 62 3E # 1 H sync offset ("31") 1F 0001111 63 3F # 1 H sync offset ("8") 1F 0001111 64 40 # 1 V sync offset ("Vsnc pulse width ("4 : 12") 41 01000001 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("344 mm") 58 01011000 68 44 # 1 H image size ("344 mm") 58 01011000 70 46 # 1 V boarder ("0") 00 0000000 71 47 Negative Shall ("186") 56 01010110 75 48 # 1 H sync offset ("58") 56 01010110 76 48 # 1 H sync offset ("68") 56 01010110 77 49 # 1 Pixel clock ("1866") 56 01010110 78 48 # 1 H sync offset ("34") 56 01010000 79 46 # 1 V boarder ("0") 00 000000000000000000000000000000	44	2C	Standard timing ID # 4		
47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 Standard timing ID # 8 01 00000001 55 34 Standard timing ID # 8 01 00000001 55 35 Standard timing ID # 8 01 00000001 56 36 VESA CVT Rev1.1) 57 39 # 1 Pixel clock (hex LSB first) 3A 00111010 58 3A # 1 H active ("1366") 56 01101010 59 3B # 1 V active ("768") 50 01000000000000000000000000000000000	45	2D	Standard timing ID # 4		
48 30 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 7 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) 55 37 # 1 Pixel clock (hex LSB first) 56 38 # 1 H active ("1366") 57 39 # 1 H blank ("194") 58 3A # 1 H active ("1366") 59 3B # 1 V active ("768") 60 3C # 1 V blank ("38") 61 3B # 1 H sync offset : V sync pulse width ("4: 12") 63 4	46	2E	Standard timing ID # 5		
49 31 Standard timing ID #6 01 00000001	47	2F	Standard timing ID # 5	01	
Solid	48	30	Standard timing ID # 6		
51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) FO 11110000 54 36 VESA CVT Rev1.1) FO 11110000 55 37 # 1 Pixel clock (hex LSB first) 3A 00111010 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("194") C2 11000010 58 3A H 1 V active : Wblank ("366") 50 01010000 59 3B # 1 V active : Wblank ("368") 26 00100110 60 3C # 1 V blank ("38") 30 00110000 61 3D # 1 L sync offset ("31") 1F 00011111 62 3E # 1 H sync offset : V sync bulse width ("4: 12") 4C 01001100 64 4D # 1 V sync offset : V sync bulse width ("4: 12") 4	49	31	Standard timing ID # 6	01	00000001
52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) F0 11110000 55 37 # 1 Pixel clock (hex LSB first) 3A 00111010 56 38 # 1 H blank ("1366") 56 01010110 57 39 # 1 H blank ("194") C2 11000010 58 3A # 1 H active : H blank ("1366:194") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768:38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync offset 'V sync bync bync bync bync bync bync bync b	50	32	Standard timing ID # 7	01	00000001
Sa Standard timing ID # 8 Detailed timing description # 1 Pixel clock ("150.88MHz", According to Set Set	51	33	Standard timing ID # 7	01	00000001
Detailed timing description # 1 Pixel clock ("150.88MHz", According to VESA CVT Rev1.1) S5 37 # 1 Pixel clock (hex LSB first) 3A 00111010 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("194") C2 11000010 58 3A # 1 H active ("1466") 50 00100000 60 3C # 1 V blank ("366") 26 00100110 60 3C # 1 V blank ("36") 26 00100110 61 3D # 1 V active ("168") 26 00100110 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync offset ("31") 41 1000001 65 41 ("31.65 : 4 : 12") 47 40 41 14 14 14 14 14 14	52	34	Standard timing ID # 8	01	0000001
54 36 VESA CVT Rev1.1) FO ITT10000 55 37 # 1 Pixel clock (hex LSB first) 3A 00111010 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("194") C2 11000010 58 3A # 1 H active : H blank ("1366 :194") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768:38") 30 00110000 62 3E # 1 H sync offset ("55") 41 01000000 64 40 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 65 41 ("31: 65 : 4 : 12") 0 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") 58 01011000 68 42 # 1 H image size ("344 mm")	53	35		01	0000001
56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("194") C2 11000010 58 3A # 1 H active : H blank ("1366 : 194") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768 : 38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 0001111 63 3F # 1 H sync offset : V sync pulse width ("4 : 12") 4C 01001100 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("31: 65 : 4 : 12") 4C 01001100 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size ("194 mm") 00 00000000 70 46	54	36		F0	11110000
57 39 # 1 H blank ("194") C2 11000010 58 3A # 1 H active : H blank ("1366 :194") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768 :38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync offset : V sync pulse width ("4 : 12") 4C 01001100 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("31: 65 : 4 : 12") 4C 01001100 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V bimage size ("194 mm") C2 11000010 68 44 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Neg	55	37	# 1 Pixel clock (hex LSB first)	3A	00111010
58 3A # 1 H active : H blank ("1366 :194") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("36") 26 00100110 61 3D # 1 V scrive : V blank ("768 :38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("31: 65 : 4 : 12") 4C 01001100 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00100000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 000000000 71 47 <	56	38	# 1 H active ("1366")	56	01010110
59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768 :38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync pulse width ("65") 41 01000100 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("31: 65 : 4 : 12") 4C 01001100 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("344 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 0010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 # 1 Pixel clock (hex LSB f	57	39	# 1 H blank ("194")	C2	11000010
60 3C # 1 V blank ("38") 26 00100110 61 3D # 1 V active : V blank ("768 :38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("31: 65 : 4 : 12") 00 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("344 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 # 1 Pixel clock (hex LSB first) 36 00110110 73 49 # 1 Pixel cloc	58	ЗА	# 1 H active : H blank ("1366 :194")	50	01010000
61 3D # 1 V active : V blank ("768 :38") 30 00110000 62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 65 41 ("31: 65 : 4 : 12") 0 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Detailed timing description # 1 Pixel clock ("138.30MHz", According to Vesatives 00001100 72 48 VESA CVT Rev1.1) 36 00110110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 75 4B <td>59</td> <td>3B</td> <td># 1 V active ("768")</td> <td>00</td> <td>00000000</td>	59	3B	# 1 V active ("768")	00	00000000
62 3E # 1 H sync offset ("31") 1F 00011111 63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 65 41 "1 H sync offset : H sync pulse width : V sync offset : V sync width ("31:65 : 4 : 12") 00 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 8 00011000 72 48 # 1 Pixel clock (hex LSB first) 36 00110110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 75 4B # 1 H blank ("194") 50 01010000 76	60	3C	# 1 V blank ("38")	26	00100110
63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("31: 65 : 4 : 12") 58 01011000 65 41 ("31: 65 : 4 : 12") 58 01011000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") 62 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 VESA CVT Rev1.1) 66 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") 50 01010000 77 4D # 1 V active : H blank ("1366 :194") 50 01000000 78 4E # 1 V blank ("38") 60 00000110 79 4F # 1 V active ("768") 79 4F # 1 V active : V blank ("768 :38") 79 4C 01001100 80 50 # 1 H sync offset : V sync pulse width ("4 : 12") 70 0000000000000000000000000000000000	61	3D	, ,	30	00110000
63 3F # 1 H sync pulse width ("65") 41 01000001 64 40 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 65 41 ("31: 65 : 4 : 12") 0 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H boarder ("0") 00 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 # 1 Pixel clock (hex LSB first) 36 00110110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 75 4B # 1 H blank ("194") 56 01010110 75 4B # 1 H blank ("194") 50 0101000 76 4C # 1 H active ("1366") 50 0101000 <td>62</td> <td>3E</td> <td># 1 H sync offset ("31")</td> <td>1F</td> <td>00011111</td>	62	3E	# 1 H sync offset ("31")	1F	00011111
# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("31: 65 : 4 : 12") 66	63	3F		41	01000001
65 41 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("31: 65 : 4 : 12") 00000000 66 42 # 1 H image size ("344 mm") 58 01011000 67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 06 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 78 4E # 1 V blank ("38") 26 00100110 <	64	40	# 1 V sync offset : V sync pulse width ("4 : 12")	4C	01001100
67 43 # 1 V image size ("194 mm") C2 11000010 68 44 # 1 H image size : V image size ("344 : 194") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 VESA CVT Rev1.1) 36 0011010 73 49 # 1 Pixel clock (hex LSB first) 36 0011011 74 4A # 1 H active ("1366") 56 0101110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 : 194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync offset : V sync pulse width ("4 : 12")	65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
68	66	42	# 1 H image size ("344 mm")	58	01011000
69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 Megatives 18 00011000 72 48 Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 06 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 4C 01001100 84 54	67	43	# 1 V image size ("194 mm")	C2	11000010
70 46 # 1 V boarder ("0") 00 00000000 71 47 Negatives 18 00011000 72 48 Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 06 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width : V sync offset : V sync width ("31:65:4:12") 4C 01001100 83 53 ("31:65:4:12") 58 01011000 <td>68</td> <td>44</td> <td># 1 H image size : V image size ("344 : 194")</td> <td>10</td> <td>00010000</td>	68	44	# 1 H image size : V image size ("344 : 194")	10	00010000
# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 73	69	45	# 1 H boarder ("0")	00	00000000
71 47 Non-interlaced, Normal, no stereo, Separate sync, H/V pol 18 00011000 72 48 Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 06 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 0001111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width : V sync offset : V sync width ("31:00) 00000000 83 53 ("31: 65 : 4 : 12") 4C 01011000 84 54 # 1 H image size ("344 mm") 58	70	46	# 1 V boarder ("0")	00	00000000
The latives Detailed timing description # 1 Pixel clock ("138.30MHz", According to VESA CVT Rev1.1) 06 00000110 06 00000110 07 49 # 1 Pixel clock (hex LSB first) 36 00110110 07 4A # 1 H active ("1366") 56 01010110 07 4B # 1 H blank ("194") C2 11000010 07 4D # 1 V active ("768") 00 00000000 07 4D # 1 V active ("768") 00 00000000 07 4F # 1 V active : V blank ("38") 26 00100110 07 4F # 1 V active : V blank ("768 :38") 30 00110000 07 4F # 1 V active : V blank ("768 :38") 30 00110000 07 07 07 07 07				10	00011000
72 48 VESA CVT Rev1.1) 06 00000110 73 49 # 1 Pixel clock (hex LSB first) 36 00110110 74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 83 53 ("31: 65 : 4 : 12") 60 01011000 84 54 # 1 H image size ("344 mm") 58 01011000	71	47		10	00011000
74 4A # 1 H active ("1366") 56 01010110 75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 4C 01001100 84 54 # 1 H image size ("344 mm") 58 01011000	72	48	, , , , , , , , , , , , , , , , , , , ,		
75 4B # 1 H blank ("194") C2 11000010 76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 4C 01001000 84 54 # 1 H image size ("344 mm") 58 01011000	73	49	# 1 Pixel clock (hex LSB first)		
76 4C # 1 H active : H blank ("1366 :194") 50 01010000 77 4D # 1 V active ("768") 00 00000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 4C 01001000 84 54 # 1 H image size ("344 mm") 58 01011000	74	4A	# 1 H active ("1366")		
77 4D # 1 V active ("768") 00 000000000 78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 000000000 84 54 # 1 H image size ("344 mm") 58 01011000					
78 4E # 1 V blank ("38") 26 00100110 79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	76	4C	,		
79 4F # 1 V active : V blank ("768 :38") 30 00110000 80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	77	4D	# 1 V active ("768")	00	00000000
80 50 # 1 H sync offset ("31") 1F 00011111 81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	78	4E	# 1 V blank ("38")	26	
81 51 # 1 H sync pulse width ("65") 41 01000001 82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	79	4F	# 1 V active : V blank ("768 :38")		
82 52 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	80	50	# 1 H sync offset ("31")	1F	
# 1 H sync offset : H sync pulse width : V sync offset : V sync width 1 H sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	81	51	# 1 H sync pulse width ("65")	41	01000001
83 53 ("31: 65 : 4 : 12") 00 00000000 84 54 # 1 H image size ("344 mm") 58 01011000	82	52		4C	01001100
5. 5. m. m. mage 3.25 (5.1. mm)	83	53		00	00000000
85 55 # 1 V image size ("194 mm") C2 11000010	84	54	# 1 H image size ("344 mm")	58	01011000
	85	55	# 1 V image size ("194 mm")	C2	11000010

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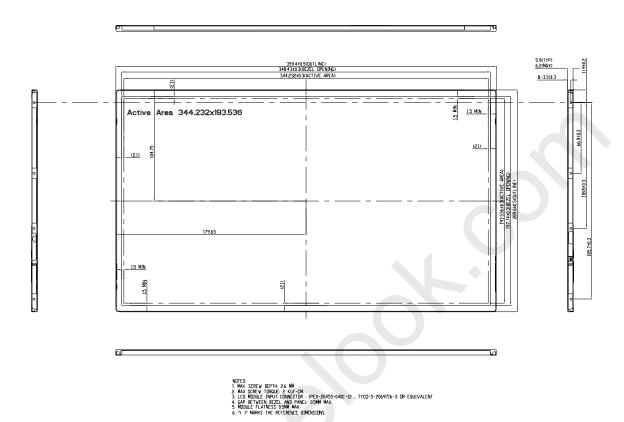
87 57 # 1 H boarder ("0") 00 0000000 88 58 # 1 Non-Interlaced, Normal, no stereo, Separate sync, H/V pol 18 00011000 89 59 # 1 Non-Interlaced, Normal, no stereo, Separate sync, H/V pol 18 00011000 90 5A Negatives 1D 00011101 91 5B P 1 Pixel clock (hex LSB first) 31 0011000 91 5C # 1 H active ("1366") 56 01010110 92 5C # 1 H active ("1366") 56 01010100 94 5E # 1 H active ("Halank ("1366 :194") 50 01000000 95 5F # 1 V active ("768") 00 0000000 96 60 # 1 V spr. offset ("3") 30 00110000 97 61 # 1 H sync pulse width ("65") 41 00000000 98 62 # 1 H sync pulse width ("65") 41 01000001 97 61 # 1 V sync offset: V sync pulse width ("4:12") 41 010000001 101	86	56	# 1 H image size : V image size ("344 : 194")	10	00010000
88 58 # 1 V boarder (°)					
S9	1		` '		
B9 59 Negatives	88	58		00	00000000
90 5A VESA CVT Rev.1.1) 91 5B #1 Pixel clock (hex LSB first) 92 5C #1 H active ("1366") 93 5D #1 H blank ("194") 94 5E #1 H active ("1366") 95 5F #1 V active ("768") 96 60 #1 V blank ("38") 97 61 #1 V blank ("38") 98 62 #1 H sync offset ("31") 99 63 #1 H sync pulse width ("65") 100 64 #1 V sync offset ("31") 101 65 ("31:65 : 4 : 12") 102 66 #1 H image size ("344 mm") 103 67 #1 H blander ("0") 106 6A #1 V blander ("0") 107 6B #1 H blander ("0") 108 6C VESA CVT Rev.1.1) 109 6B #1 H active ("1366") 110 6C #1 H blander ("1366") 111 6F #1 H active ("1366") 112 70 #1 H active ("1366") 113 71 #1 V active ("0") 114 6F #1 H active ("1366") 115 73 #1 V active ("136") 116 74 #1 H sync pulse width ("1366") 117 75 #1 H active ("136") 118 76 #1 H active ("1366") 119 77 ("136") 110 6E #1 H active ("1366") 110 6E #1 H active ("1366") 111 6F #1 H blank ("1366") 111 6F #1 H blank ("1366") 112 70 #1 H active ("1366") 113 71 #1 V active ("768") 114 72 #1 H blank ("1366") 115 73 #1 V active ("768") 116 74 #1 H active ("1366") 117 75 #1 H active ("1366") 118 76 #1 H blank ("1366") 119 77 ("136") 110 77 ("136") 111 75 #1 H active ("1366") 111 75 #1 H active ("1366") 112 70 #1 H active ("1366") 113 71 #1 V active ("768") 114 72 #1 H blank ("1366") 115 73 #1 V active ("768") 116 74 #1 H sync pulse width ("4 : 12") 117 75 #1 H active ("1366") 118 76 #1 V active ("768") 119 77 ("31:65 : 4 : 12") 110 0000000000000000000000000000000000	89	59	Negatives	18	00011000
92 SC #1 H active ("1366") 56 01010110 93 5D #1 H blank ("194") C2 11000010 94 5E #1 H active : H blank ("1366:194") 50 01010000 95 5F #1 V active ("768") 00 00000000 96 60 #1 V blank ("38") 26 00100110 97 61 #1 V active : V blank ("768:38") 30 00110000 98 62 #1 H sync offset ("31") 1F 00011111 99 63 #1 H sync pulse width ("65") 41 01000001 100 64 #1 V sync offset : V sync pulse width ("4:12") 4C 0100110 101 65 ("31:65:4:12") 58 01011000 102 66 #1 H image size ("344 mm") 58 010110001 103 67 #1 V image size ("194 mm") C2 11000010 105 69 #1 H boarder ("0") 00 00000000 106 6A #1 V boarder ("0") 00 00000000 107 6B Negatives 108 6C VESA CVT Rev1.1) 10 0011101 109 6D #1 Pixel clock (hex LSB first) 10 0011101 110 6F #1 H blank ("194") C2 11000010 111 6F #1 H blank ("196") 50 01011010 112 70 #1 H active : H blank ("1366:194") 50 01011001 113 71 #1 V active : V blank ("68") 50 01011001 114 72 #1 V blank ("38") 50 01011001 115 73 #1 V active : V blank ("68") 50 01011001 116 74 #1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives 110 0101101 111 6F #1 H blank ("194") C2 11000010 112 70 #1 H active : H blank ("1366:194") 50 01011001 113 71 #1 V active ("1366") 56 01011010 114 72 #1 V blank ("38") 50 0000000000000000000000000000000000	90	5A			
93 5D # 1 H blank ("194") 50 10100000 94 5E # 1 H active : H blank ("1366:194") 50 01010000 95 5F # 1 V active ("768") 00 00000000 96 60 # 1 V blank ("38") 26 00100110 97 61 # 1 V active : V blank ("768:38") 30 00110000 98 62 # 1 H sync offset ("31") 1F 0001111 99 63 # 1 H sync offset : V sync pulse width ("65") 41 01000001 100 64 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 101 65 ("31:65:4:12") 58 01011000 102 66 # 1 H image size ("344 mm") 58 01011000 103 67 # 1 V image size ("194 mm") 58 01011000 105 69 # 1 H boarder ("0") 00 00000000 106 6A # 1 V boarder ("0") 00 000000000000000000000000000000	91	5B	# 1 Pixel clock (hex LSB first)	31	
94 5E #1 H active : H blank ("1366 :194") 50 01010000 95 5F #1 V active ("768") 00 00000000 96 60 #1 V blank ("38") 26 00100110 97 61 #1 V active : V blank ("768 :38") 30 00110000 98 62 #1 H sync offset ("31") 1F 00011111 99 63 #1 H sync offset : V sync pulse width ("4 : 12") 4C 01001100 100 64 #1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 101 65 ("31: 65 : 4 : 12") 58 01011000 102 66 #1 H limage size ("344 mm") 58 0111000 103 67 #1 V image size ("194 mm") 58 01111000 104 68 #1 H image size : V image size ("344 : 194") 10 0000000 105 69 #1 H boarder ("0") 00 00000000 106 6A #1 V boarder ("0") 00 00000000 107 6B Negatives 054 054 054 054 054 054 054 054 054 054	92	5C	# 1 H active ("1366")	56	01010110
95 5F #1 V active ("768") 00 0000000 96 60 #1 V blank ("38") 26 00100110 97 61 #1 V active : V blank ("768 :38") 30 00100110 98 62 #1 H sync offset ("31") 1F 00011111 99 63 #1 H sync pulse width ("65") 41 01000001 100 64 #1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 101 65 ("31 :65 : 4 : 12") 58 01011000 102 66 #1 H image size ("344 mm") 58 01011000 103 67 #1 V image size ("144 mm") 58 01011000 104 68 #1 H boarder ("0") 00 00000000 105 69 #1 H boarder ("0") 00 00000000 106 6A #1 V boarder ("0") 00 000000000000000000000000000000	93	5D	# 1 H blank ("194")	C2	11000010
96 60 #1 V blank ("36") 26 00100110 97 61 #1 V active: V blank ("768:38") 30 00110000 98 62 #1 H sync offset ("31") 1F 00011111 99 63 #1 H sync pulse width ("65") 41 10000001 100 64 #1 V sync offset: V sync pulse width ("4:12") 4C 01001100 110	94	5E	# 1 H active : H blank ("1366 :194")	50	01010000
97 61 #1 V active: V blank ("768:38") 98 62 #1 H sync offset ("31") 99 63 #1 H sync pulse width ("65") 100 64 #1 V sync offset: V sync pulse width ("4:12") 40 0000000 101 65 ("31:65:4:12") 102 66 #1 H image size ("344 mm") 103 67 #1 V image size ("194 mm") 104 68 #1 H image size: V image size ("344:194") 107 68 Negatives 108 60 V ESA CVT Rev1.1) 109 60 #1 Pixel clock (hex LSB first) 110 6E #1 H active ("1366") 111 6F #1 H blank ("194") 112 70 #1 H active ("168") 113 71 #1 V active ("768") 114 72 #1 V image size ("344 mm") 115 73 #1 V sactive ("768") 116 74 #1 H sync offset: V sync pulse width ("4:12") 117 75 #1 H sync offset: V blank ("768:38") 118 76 #1 V sync offset: V blank ("65") 119 77 ("31:55:4:12") 110 00000000 120 78 #1 H boarder ("31") 121 79 #1 H image size: V image size ("344:194") 122 78 #1 H image size: V image size ("544:194") 123 78 #1 H sync offset: V sync pulse width ("4:12") 124 76 #1 H sync offset: V sync pulse width ("4:12") 125 77 #1 H image size: V image size ("344:194") 126 77 #1 H image size: V image size ("344:194") 127 78 #1 H sync offset: V sync pulse width ("4:12") 128 77 #1 H image size: V image size ("344:194") 129 78 #1 H limage size: V image size ("344:194") 120 78 #1 H limage size ("344 mm") 121 79 #1 V image size ("344 mm") 122 77 #1 H image size ("344 mm") 123 78 #1 H image size: V image size ("344:194") 124 77 #1 H boarder ("0") 125 78 #1 H boarder ("0") 126 77 Ketzive: V image size ("344 mm") 127 78 #1 H boarder ("0") 128 78 #1 H image size: V image size ("344:194") 129 79 #1 V image size: V image size ("344:194") 120 0000000000000000000000000000000000	95	5F	# 1 V active ("768")	00	00000000
98 62 #1 H sync offset ("31")	96	60	# 1 V blank ("38")	26	00100110
99 63 #1 H sync pulse width ("65") 41 01000001 100 64 #1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 #1 H sync offset : H sync pulse width : V sync offset : V sync width 65 ("31: 65 : 4 : 12") 00 00000000 102 66 #1 H image size ("194 mm") 58 01011000 103 67 #1 V image size ("194 mm") C2 11000010 104 68 #1 H image size : V image size ("344 : 194") 10 00010000 105 69 #1 H boarder ("0") 00 00000000 106 6A #1 V boarder ("0") 00 00000000 107 6B Negatives 01 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives 0111000 108 6C VESA CVT Rev1.1) 10 00011000 109 6D #1 Pixel clock (hex LSB first) 1D 00011101 110 6E #1 H active ("1366") 56 010101101 121 70 #1 H active : H blank ("1366 : 194") 50 0100000001 133 71 #1 V active ("768") 00 000000000000000000000000000000000	97	61	# 1 V active : V blank ("768 :38")	30	00110000
100	98	62	# 1 H sync offset ("31")	1F	00011111
# 1 H sync offset : H sync pulse width : V sync offset : V sync width 101 65 ("31: 65: 4: 12")	99	63	# 1 H sync pulse width ("65")	41	01000001
101 65 ("31: 65 : 4 : 12") 00 00000000 102 66 # 1 H image size ("344 mm") 58 01011000 103 67 # 1 V image size ("194 mm") C2 11000010 104 68 # 1 H boarder ("0") 00 00000000 105 69 # 1 H boarder ("0") 00 00000000 106 6A # 1 V boarder ("0") 00 00000000 107 6B Negatives 18 00011000 108 6C VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 00011010 110 6E # 1 H active ("1366") 1D 00011011 110 6E # 1 H blank ("194") C2 11000010 112 70 # 1 H active : H blank ("1366:194") 50 01010000 113 71 # 1 V active : V blank ("768") 00 00000000 114 72 # 1 V blank ("38") 30 00110000	100	64		4C	01001100
103 67 # 1 V image size ("194 mm") C2 11000010 104 68 # 1 H image size : V image size ("344 : 194") 10 00010000 105 69 # 1 H boarder ("0") 00 00000000 106 6A # 1 V boarder ("0") 00 00000000 107 6B Negatives 18 00011000 108 6C Detailed timing description # 1 Pixel clock ("75.44MHz", According to VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 00011101 110 6E # 1 H active ("1366") 56 01010110 111 6F # 1 H blank ("194") C2 11000010 112 70 # 1 H active ("768") 90 00000000 113 71 # 1 V active ("768") 90 000000000 114 72 # 1 V blank ("38") 26 00100110 115 73 # 1 V scrive : V blank ("768 :38") 30 00110000 116 74 #	101	65		00	00000000
103 67 # 1 V image size ("194 mm") C2 11000010 104 68 # 1 H image size : V image size ("344 : 194") 10 00010000 105 69 # 1 H boarder ("0") 00 00000000 106 6A # 1 V boarder ("0") 00 00000000 107 6B Megatives 18 00011000 108 6C VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 00011101 110 6E # 1 H active ("1366") 56 01010110 111 6F # 1 H blank ("194") C2 11000010 112 70 # 1 A active ("768") 00 00000000 113 71 # 1 V blank ("38") 26 00100110 115 73 # 1 V sctive : V blank ("768 :38") 30 00110000 116 74 # 1 H sync offset ("65") 41 01000001 118 76 # 1 V sync offset : V sync pulse width ("4 : 12") 4	102	66	# 1 H image size ("344 mm")	58	01011000
105 69 # 1 H boarder ("0") 00 00000000 106 6A # 1 V boarder ("0") 00 00000000 107 6B # 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives 18 00011000 108 6C Detailed timing description # 1 Pixel clock ("75.44MHz", According to VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 0001101 110 6E # 1 H active ("1366") 56 01010110 111 6F # 1 H blank ("194") C2 11000010 112 70 # 1 H active : H blank ("1366 :194") 50 01010000 113 71 # 1 V active ("768") 00 00000000 114 72 # 1 V blank ("38") 26 00100110 115 73 # 1 V active : V blank ("768 :38") 30 0011000 116 74 # 1 H sync pulse width ("65") 1F 00011111 117 75 # 1 H sync pulse width ("4 : 12") 4C 01001100 <td>103</td> <td>67</td> <td>_ ,</td> <td>C2</td> <td>11000010</td>	103	67	_ ,	C2	11000010
106 6A # 1 V boarder ("0") 00 00000000 107 6B # 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives 18 00011000 108 6C VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 00011101 110 6E # 1 H active ("1366") 56 01010110 111 6F # 1 H blank ("194") C2 11000010 112 70 # 1 H active : H blank ("1366 :194") 50 01010000 113 71 # 1 V active : H blank ("768") 00 00000000 114 72 # 1 V blank ("38") 26 00100110 115 73 # 1 V active : V blank ("768 :38") 30 00110000 116 74 # 1 H sync offset ("31") 1F 00011111 117 75 # 1 H sync pulse width ("65") 41 01000001 118 76 # 1 V sync offset : V sync pulse width ("4 : 12") 4C 01001100 119	104	68	# 1 H image size : V image size ("344 : 194")	10	00010000
# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives Detailed timing description # 1 Pixel clock ("75.44MHz", According to VESA CVT Rev1.1) 109 6D # 1 Pixel clock (hex LSB first) 110 6E # 1 H active ("1366") 111 6F # 1 H blank ("194") 112 70 # 1 H active : H blank ("1366 :194") 113 71 # 1 V active ("768") 114 72 # 1 V blank ("38") 115 73 # 1 V active : V blank ("768 :38") 116 74 # 1 H sync offset ("31") 117 75 # 1 H sync offset : V sync pulse width ("4 : 12") 118 76 # 1 V sync offset : H sync pulse width : V sync offset : V sync width 119 77 ("31: 65 : 4 : 12") 120 78 # 1 H image size ("344 mm") 121 79 # 1 V image size ("194 mm") 122 7A # 1 H image size : V image size ("344 : 194") 125 7D Restance of the control	105	69	# 1 H boarder ("0")	00	00000000
107 6B Negatives 18 00011000 108 6C Detailed timing description # 1 Pixel clock ("75.44MHz", According to VESA CVT Rev1.1) 78 01111000 109 6D # 1 Pixel clock (hex LSB first) 1D 00011101 110 6E # 1 H active ("1366") 56 01010110 111 6F # 1 H blank ("194") 50 01010000 113 71 # 1 V active : H blank ("1366:194") 50 01010000 113 71 # 1 V blank ("38") 26 00100110 115 73 # 1 V active : V blank ("768:38") 30 00110000 116 74 # 1 H sync offset ("31") 1F 00011111 117 75 # 1 H sync pulse width ("65") 41 01000001 118 76 # 1 V sync offset : V sync pulse width : V sync offset : V sync width ("31:65:4:12") 4C 01001100 119 77 ("31:65:4:12") 4C 01001000 120 78 # 1 H image size ("344 mm") 58 01011000	106	6A	# 1 V boarder ("0")	00	00000000
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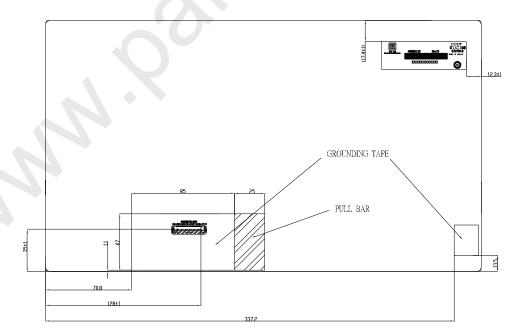
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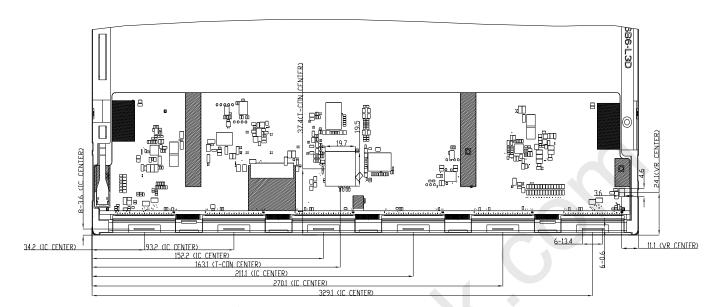
Appendix. OUTLINE DRAWING





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MOTES:

1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAM OR OTHER FOREIGN OBJECTS OVER TOON AND VR LOCATION.

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